IN THE SPECIFICATION

Please replace the paragraph at page 9, line 23 beginning with "After gate dielectric layer 120" as follows:

C1

After gate dielectric layer 120 is formed, **Figure 2** shows the substrate of **Figure 1** after the further processing step of depositing metal layer 130 over the surface of substrate 100. In this embodiment, metal layer 130 is deposited to a thickness of, for example, 500 – 2000 Å. In the embodiments that are described herein, the physical properties of at least a portion of metal layer 130 will be modified to adjust the work function for optimum NMOS and PMOS device performance. Thus, metal layer 130 will serve in its present state or in a modified state as a gate electrode. Accordingly, the thickness of metal layer 130 is scalable and should be chosen based primarily on integration issues related to device performance. Further, since in many of the embodiments that are described herein, the physical properties of metal layer 130 will be modified, care should be taken to avoid making metal layer 132 too thick so that, when desired, any modification or transformation of metal layer 130 is complete.

Please replace four consecutive paragraphs starting at page 14, line 18, beginning with "**Figures 8-11** illustrate a second process" as follows:

C2

Figures 8-11 illustrate a second process of forming complementary gate electrodes for optimum NMOS and PMOS device performance. In this process, as shown in **Figure 8**, semiconductor substrate or epitaxial layer 100 of a substrate has N-type well 105 and P-type well 115 formed in substrate or epitaxial layer 100 defining active area or cell region by shallow trench isolation structures 110. Overlying substrate 100 is gate dielectric 120 as described above and metal layer 130 deposited to a scalable thickness of, for example, approximately 500-2000 Å. In one embodiment, metal layer 130 is chosen to have an appropriate work function for one of an NMOS gate electrode

and a PMOS gate electrode (e.g., about 4.1 electrons-volts or 5.2 electron-volts, respectively). Alternatively, metal layer 130 may require subsequent modification to tune the material to an appropriate work function for a PMOS device. Deposited over metal layer 130 in **Figure 8** is second metal or other material layer 160.

Figure 9 shows the structure after the further processing step of patterning second metal or other material layer 160 over a portion of metal layer 130. In this case, second metal layer 160 is patterned over the active area or cell region denoted by P-type well 115. Metal layer 130 overlying N-type well 105 is left exposed.

Next, the structure is exposed to a heat treatment, such as for example, a high temperature (e.g., 900-1000°C) or laser anneal, to drive the reaction or combination of second metal or other material layer 160 and metal layer 130 to form a metal alloy or other compound. **Figure 10** shows substrate 100 after the further processing step of subjecting metal layer 130 to a heat treatment and forming a metal alloy or other metal compound over P-type well 115. The metal alloy or metal compound 165 is selected to have an appropriate work function for an NMOS device. Examples of suitable metal alloys or metal compounds formed in the manner described include, but are not limited to, molybdenum silicide.

Figure 11 shows substrate 100 after the further processing step of patterning metal layers 130 and 165 into metal gate electrodes and forming PMOS transistor device 161 and NMOS transistor device 162 by a process such as described above with reference to **Figures 6** and **7**. PMOS transistor device 161 includes doped diffusion or junction regions 170 and NMOS transistor device 162 includes doped diffusion or junction regions 175. Finally, as an example, **Figure 11** illustrates the coupling of PMOS device 161 and NMOS device 162 for an inverter.